WHAT IS CLAIMED IS:

1. A stacked semiconductor device, comprising:

a substrate having a conductor pattern and a die bonding portion, wherein the conductor pattern has pads;

a first die bonded on the die bonding portion of the substrate and having pads thereon, wherein the pads of the first die are electrically connected to the pads of the conductor pattern by wires;

a first adhesive layer provided on the substrate to cover the first die and the wires, wherein the first adhesive layer has a top, and

a second die bonded on the top of the first adhesive layer and having pads thereon, wherein the pads of the second die are electrically connected to the pads of the conductor pattern by wires.

2. The stacked semiconductor device as defined in claim 1, further comprising a second adhesive layer provided on the substrate to cover the second die and the wires.

3. The stacked semiconductor device as defined in claim 1, wherein a size of the top of the first adhesive layer is greater than a size of a top of the first die.

4. The stacked semiconductor device as defined in claim 1, wherein a size of the top of the first adhesive layer is substantially equal to a size of a bottom of the second die.

5. The stacked semiconductor device as defined in claim 1, wherein a size of the first die is smaller than a size of the second die.

6. A stacked semiconductor device, comprising:

a substrate having a conductor pattern and a die bonding portion, wherein the conductor pattern has pads;

a first die bonded on the die bonding portion of the substrate and having pads thereon, wherein the first die is electrically connected to the pads of the conductor pattern;

a first adhesive layer provided on the substrate to cover the first die, wherein the first adhesive layer has a top and the top thereof is greater than the first die, and

a second die bonded on the top of the first adhesive layer and electrically connected to the pads of the conductor pattern, wherein the second die is greater than the first die.

7. The stacked semiconductor device as defined in claim 6, further comprising a second adhesive layer provided on the substrate to cover the second die.

8. The stacked semiconductor device as defined in claim 7, wherein the second die is electrically connected to the pads of the conductor pattern by wires and the second adhesive layer covers both of the second die and the wires.

9. The stacked semiconductor device as defined in claim 6, wherein the first die is electrically connected to the pads of the conductor pattern by wires and the first adhesive layer covers both of the first die and the wires.

10. The stacked semiconductor device as defined in claim 6, wherein a size of the to of the first adhesive layer is substantial equal to a size of a bottom of the second die.